ABSTRACT OF THE DISCLOSURE

Memory cells each having a floating gate (4), control gate (6), and source and drain diffusion layers (7a, 7b) are formed on a silicon substrate (1). A silicon nitride film (10) by low-pressure CVD is maintained as side wall insulating films on side walls of the gates in each memory cell. A silicon nitride film (11) by plasma CVD is formed to cover a memory cell array, and silicon oxide films (12a, 12b) are made on the silicon nitride film (11) to form an inter-layer insulating film. A common source line (13) connected to the source diffusion layer 7a is formed to embed in the silicon oxide film (12a), and a bit line (14) connected to the drain diffusion layer (7b) is formed on the silicon oxide film (12b).